In the Claims

Amend claims 1-16 as follows:

1. (Currently Amended) A memory system comprising:

a plurality of DRAMs having circuits to accept non-inverted input signals and inverted input signals~~.~~;

a register programmed to provide inverted or non-inverted signals to the DRAMS; and

programmable pins in the register and the DRAMs to enable operation in either non-inverted or inverted mode, wherein one programmable pin is connected to ground to provide one mode and the other programmable pin is connected to Vdd to operate in the other mode.

2. (Original) The memory system of claim 1 which includes re-drive circuitry, which can output both non-inverted and inverted polarity signals from one or more input signals.

3. (Canceled)

4. (Currently Amended) ~~A~~ The memory system according to claim ~~3~~ 1 wherein the DRAMs are mounted on a DIMM.

5. (Canceled)

6. (Original) A memory system comprising:

a plurality of DRAMs having circuits to accept non-inverted input signals and inverted input signals; and

a memory controller which can drive either non-inverted or inverted signals to the DRAMs using a programmable pin.

7. (Currently Amended) ~~A~~ The memory system according to claim 6 wherein the memory controller may operate in ~~one~~ a first mode at powerup and a second mode ~~means for changing modes~~ after powerup as configured by a logic element integral to the memory controller that is responsive to the programmable pin.

8. (Original) The memory system of claim 6 wherein the pin is hard-wired to the DRAMs.

9. (Original) A memory system of claim 1 in which the register drives either non-inverted or inverted signals to the DRAMs using a programmable pin.

10. (Currently Amended) A memory system comprising:

a module having a plurality of DRAMs with inputs and outputs and circuits to accept either non-inverted input signals and inverted input signals, wherein pre-selected DRAMs may operate in the inverted mode with some critical signals remaining in a non-inverted mode;

a means connected to the circuits for changing modes to accept inverted input signals; ~~and~~

a memory controller which is programmable to operate in non-inverted mode at power up and to change after it is programmed.

11. (Canceled)

12. (Original) The memory system of claim 10 wherein the memory controller may operate in the inverted mode with some critical signals remaining in non-inverted mode.

13. (Original) The memory system of claim 10 wherein a programmable pin is hard-wired to the module.

14. (Original) The memory system of claim 10 wherein the means for changing modes includes a pin that is controlled by the memory controller.

15. (Original) A DIMM comprising:

a plurality of DRAMs with means for operating with non-inverted or inverted signals based on a pre-selected operating mode; and

signal re-drive circuitry which generates an output in both non-inverted and inverted polarity signals from one or more input signals.

16. (Original) A computer system with a memory system comprising:

memory devices and re-drive circuitry external to the said memory devices, said re-drive circuitry having means for outputting both non-inverted and inverted polarity signals from one or more input signals, and said memory devices designed to operate with non-inverted or inverted signals based on a selected operating mode.